CLAIM AMENDMENTS

Please amend the pending claims as follows:

1. (currently amended) A media processor, implemented as a system on a chip, for the processing of media based upon instructions, comprising:

a plurality of processing layers wherein each processing layer has at least one processing unit, at least one program memory, and at least one data memory, each of said processing unit, program memory, and data memory being in communication with one another;

at least one processing unit in at least one of said processing layers performing line echo cancellation functions on received data;

at least one processing unit in at least one of said processing layers performing encoding or decoding functions on received data; and

a task scheduler adapted to receive a plurality of tasks from a source and distributing said tasks to said processing layers.

2. (original) The media processor of claim 1 further comprising a direct memory access controller for handling data transfers, each of said transfers having a size and a direction, from at least one data memory having an address and a plurality of external memory units, each having an address.

3. (original) The media processor of claim 2 wherein said transfers between at least one data memory and at least one external memory occur by utilizing the address of the data memory, the address of the external memory, the size of the transfer, and the direction of the transfer.

4. (original) The media processor of claim 1 wherein the task scheduler is in communication with an external memory.

5. (original) The media processor of claim 1 further comprising an interface for the receipt and transmission of data and control signals.

6. (original) The media processor of claim 5 wherein the interface comprises a UTOPIA compatible interface.

7. (original) The media processor of claim 5 wherein the interface comprises a time division multiplex compatible interface.

8. (original) The media processor of claim 1 wherein at least one processing layer includes a processing unit performing line echo cancellation functions on received data and a processing unit designed performing encoding or decoding functions on received data and wherein said line echo cancellation and encoding or decoding functions are performed in a pipelined manner.

9. (original) The media processor of claim 1 wherein the processing unit designed to perform encoding or decoding functions comprises an arithmetic and logic unit, multiply and accumulate unit, barrel shifter, and normalization unit.

10. (original) The media processor of claim 1 wherein the processing unit additionally performs voice activity detection and tone signaling functions.

11. (original) The media processor of claim 10 wherein the processing unit comprises a plurality of single-cycle multiply and accumulate units operating with an address generation unit and an instruction decoder.

12. (currently amended) A media gateway for the processing of data and communication of data across a plurality of networks, comprising:

a plurality of media processors, each of said media processors having a plurality of processing layers wherein each processing layer has at least one processing unit, at least one program memory, and at least one data memory, each of said processing unit, program memory, and data memory being in communication with one another, wherein at least one processing unit in at least one of said processing layers performs echo cancellation functions on received data, wherein at least one processing unit in at least one of said processing layers performs encoding or decoding functions on received data, and wherein a task scheduler is adapted to receive a plurality of tasks from a source and distributing said tasks to the processing layers and wherein each of said processing layers and task scheduler is implemented together as a system on chip;

a plurality of packet processors in communication with at least one of said media processors wherein the packet processor is adapted to

packetize processed data; and

a host processor in communication with at least one said packet or media processors.

13. (currently amended) A method for processing media based upon instructions, comprising the steps of:

receiving said media through a data interface;

scheduling the processing of said media through a task scheduler adapted to receive a plurality of tasks from a source and distributing said tasks to a plurality of processing layers; and

processing said media in the plurality of processing layers wherein each processing layer has at least one processing unit, at least one program memory, and at least one data memory, each of said processing unit, program memory, and data memory being in communication with one another wherein each of said receiving, scheduling, and processing steps occurs in a processor implemented as a system on a chip.

14. (original) The method of claim 13 wherein said processing step further comprises performing echo cancellation functions on received data.

15. (original) The method of claim 13 wherein said processing step further comprises performing encoding or decoding functions on received data;

16. (original) The method of claim 13 wherein the processing step occurs in parallel across multiple processing layers, each of said processing layers having similar processing units.

17. (original) The method of claim 13 wherein at least one processing layer includes a processing unit performing echo cancellation functions on received data and a processing unit performing encoding or decoding functions on received data and wherein said echo cancellation and encoding or decoding functions are performed in a pipelined manner.

18. (Canceled)

19. (currently amended) A processor for the processing of data based upon instructions, comprising:

a plurality of processing layers wherein each processing layer has at least one processing unit, at least one program memory, and at least one data memory, each of said processing unit, program memory, and data memory being in communication with one another; and

a task scheduler capable of receiving a plurality of tasks from a source and distributing said tasks to the processing layers wherein each of said processing layers and task scheduler is implemented in a single system on chip.

20. (original) The processor of claim 19 wherein at least one processing layer comprises a processing unit performing echo cancellation functions on received data.

21. (original) The processor of claim 19 wherein at least one processing layer comprises a processing unit performing encoding or decoding functions on received data.

22. (original) The processor of claim 19 wherein the processing layers communicate with task scheduler through a controller interface.